Notice of Allowability	Application No.	Applicant(s)	
	10/628,498	OSAWA ET AL.	
	Examiner	Art Unit	
	Gary Mui	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/07/2007*.

2. ☒ The allowed claim(s) is/are *2-5,7-9,12,13,15-17 and 19-32 (renumbered 1-26)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

11.30.2007

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

Drawings

1. The drawings were received on September 7, 2007. These drawings are acceptable.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance:

Claim 2 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; and a reference table that holds, among transmission delay values between the individual ports, maximum values corresponding to different combinations of active ports, wherein a value read out from the reference table according to an output signal of the status checker is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 3 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; and a reference table that holds whichever are larger between, among transmission delay values between the individual ports, maximum values corresponding to different combinations of active ports and, among transmission delay values required for the individual ports to handle signal input and output singly, maximum values corresponding to different combinations of active ports,, wherein a value read out from the reference table according to an output signal of the status

checker is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 4 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; and a reference table that holds, for each of the ports, whichever are larger between, among transmission delay values between the ports excluding that port, maximum values corresponding to different combinations of active ports and a transmission delay value required for that port to handle signal input and output singly, wherein a value read out from the reference table according to an output signal of the status checker and input port information obtained from the bus arbitration circuit is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 5 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose a reference table that holds whichever are larger between maximum transmission delay values between the individual ports and maximum transmission delay values required for the individual ports to handle signal input and output singly, wherein a value read out from the reference table is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register.

Claim 7 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing

processor includes: a status checker that checks for active individual ports; and a delay setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register and that, according to a result of the checking, assigns a transmission delay value stored in the second register to the first register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 8 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; and a delay setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a transmission delay value stored in the second register to the first register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 9 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; and a delay setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a transmission delay value stored in the second register to a reply packet returned to the external

node. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 12 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; and a reference table that holds, among jitter values between the individual ports, maximum values corresponding to different combinations of active ports, wherein a value read out from the reference table according to an output signal of the status checker is assigned, as the jitter value of the transmitter/receiver apparatus, to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 13 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; and a reference table that holds, for each of the ports, among jitter values between that port and the other ports, maximum values corresponding to different combinations of active ports, wherein a value read out from the reference table according to an output signal of the status checker and input port information obtained from the bus arbitration circuit is assigned, as the jitter value of the transmitter/receiver apparatus, to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 15 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; and a jitter setter

that checks for a type of active ports by referring to an output signal of the status checker and to the second register and that, according to a result of the checking, assigns a jitter value stored in the second register to the first register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 16 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; and a jitter setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a jitter value stored in the second register to the first register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 17 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks whether the individual ports are active or not; and a jitter setter that checks type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a jitter value stored in the second register to a reply packet returned to the

external node. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 19 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds transmission delay values between the individual ports; and a delay selector that selects, according to an output signal of the status checker, a maximum transmission delay value between active ports from among all the transmission delay values stored in the reference table, and that then assigns the selected value to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 20 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds transmission delay values between the individual ports and transmission delay values required for the individual ports to handle signal input and output singly; and a delay selector that selects, according to an output signal of the status checker, a maximum transmission delay value involving an active port from among all the transmission delay values stored in the reference table, and that then assigns the selected value to the register. delay values stored in the reference table, and that then assigns the selected value to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 21 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds transmission delay values between the individual ports and transmission delay values required for the individual ports to handle signal input and output singly; and a delay selector that selects, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a largest of transmission delay values between active ports other than a signal input port and a transmission delay value required for the signal input port to handle signal input and output singly from among all the transmission delay values stored in the reference table, and that then assigns the selected value to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 22 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds jitter values between the individual ports; and a jitter selector that selects, according to an output signal of the status checker, a maximum jitter value between active ports from among all the jitter values stored in the reference table, and that then assigns the selected value to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 23 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing

processor includes: a status checker that checks for active individual ports; a reference table that holds jitter values between the individual ports; and a jitter selector that selects, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a maximum jitter value between a signal input port and other active ports from among all the jitter values stored in the reference table, and that then assigns the selected value to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 24 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds, for each of the ports, a transmission delay value through that port and through a signal format converter for that port; and a delay calculator that selects, according to an output signal of the status checker, two largest from among transmission delay values through active ports stored in the reference table, that then adds together the two values and a maximum transmission delay value required for signal processing in a physical layer, and that then assigns a sum thereof to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 25 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose a delay calculator that compares a transmission delay value obtained by adding together two largest of the transmission delay values stored in the reference table with a transmission delay value required for a given port to handle signal input and output singly, that then adds to whichever of the two values is

larger a maximum transmission delay value required for signal processing in a physical layer, and that then assigns a sum thereof to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 26 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the delay value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds, for each of the ports, a transmission delay value through that port and through a signal format converter for that port; and a delay calculator that compares, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a transmission delay value obtained by adding together two largest of transmission delay values through active ports excluding a signal input port stored in the reference table with a transmission delay value required for the signal input port to handle signal input and output singly, that then adds to whichever of the two values is larger a maximum transmission delay value required for signal processing in a physical layer, and that then assigns a sum thereof to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 27 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds, for each of the ports, a jitter value through that port and through a signal format converter for that port; and a jitter calculator that selects, according to an output signal of the status checker, two largest from among jitter values through active ports stored in the

reference table, that then adds together the two values and a maximum jitter value required for signal processing in a physical layer, and that then assigns a sum thereof to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Claim 28 is allowable over the prior art of record since the cited reference references taken individually or in combination fails to particularly disclose the jitter value optimizing processor includes: a status checker that checks for active individual ports; a reference table that holds, for each of the ports, a jitter value through that port and through a signal format converter for that port; and a jitter calculator that adds together, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a jitter value required for a signal input port to handle signal input and output singly, a maximum jitter value through active ports excluding the signal input port stored in the reference table, and a maximum jitter value required for signal processing in a physical layer, and that then assigns a sum thereof to the register. Therefore, the prior art of record fails to show or render obvious the above underline limitations as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary Mui whose telephone number is (571) 270-1420. The examiner can normally be reached on Mon. - Thurs. 9 - 3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GM 11.20.2007